directed to a synapse MOS transistor for use in a neural network. The synapse MOS transistor in Chung describes gate electrodes of different lengths, different widths or different lengths and widths. (See Chung Abstract). Austin appears to describe a static low-power differential sense amplifier circuit. The Austin reference does not allude to or suggest any teaching to neural networks. Further, the Austin reference makes no mention and does not address any purpose of saving space such that one would look to the space saving advantages described in Chung. In sum, the differential sense amplifier art discussed in Austin is altogether non-analogous art to the Chung reference for neural networks.

In the Applicant's "Background of the Invention" section, the Applicant lays forth the following problem associated with the operational speed in low power supply sense amplifiers:

> Lower and lower power supply voltages are being employed on DRAM memory chips, which places more stringent requirements on the design parameters of sense amplifiers. It is difficult to get a conventional sense amplifier to have adequate response characteristics at these lower power supply voltages. Figure 1A is a schematic diagram illustrating a conventional cross-coupled sense amplifier. Figure 1B is a graph illustrating the very slow response of the conventional cross-coupled sense amplifier at a power supply voltage of 0.5V. As shown in Figure 1B, it can take up to nearly 100 nanoseconds (t = 100 ns) to achieve a significant sense signal and output voltage from the sense amplifier. This is far too long to be of any use in a conventional memory system.

To address this problem, the Applicant's invention describes and claims the use of a dual gated MOS in a novel latch, amplifier, or sense amplifier. The Austin reference does not address operational speed concerns anywhere within the reference. Nor does the Chung reference address operational speed concerns, and is not even directed to differential sense amplifiers.

That is, Applicant's independent claim 10, as well as each of the Applicant's other independent claims, cites using a dual-gated metal oxide semiconductor. As explained in detail in the Applicant's specification, the use of the dual-gated metal oxide semiconductor in the Applicant's novel amplifier or latch allows the device to obtain a much faster response time for obtaining a full output sense voltage since the output nodes only need to drive the small stray capacitances of the nodes, V1 and V2 (see Figure 2A), and the input capacitances of the

subsequent amplifiers. (See specification page 13, ln. 29 through page 14, ln. 2). As stated on page 11, ln. 10 of the Applicant's specification, the "novel sense amplifier of the present invention has a much faster response time of less than 10 nanoseconds (t=10 ns)." Arguably, the same could not be achieved without the Applicant's novel structure as claimed. The physics of this novel structure are explained in detail in connection with Figure 2C, beginning on line 12, page 11 of the specification through page 14, line 13.

Since the Austin reference does not address speed concerns, there is no motivation from within the reference to consider dual-gated metal oxide transistors. Further, since the Chung reference addresses neither differential sense amplifiers nor speed issues, there is no motivation from within the reference to consult the Austin reference.

Thus, the assertion made in Section 2 of the office action is based on hindsight, and is not in accordance with M.P.E.P. §§706.02 and 2143, which states:

> The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure. and "The level of skill in the art cannot be relied upon to provide the suggestion to combine references." *Al-Site Corp. v. VSI Int'l Inc.*, 174 F.3d 1308, 50 USPQ2d 1161 (Fed. Cir. 1999).

Therefore, combining the Austin and Chung references is improper.

Furthermore, claim 13 recites "the pair of input transmission line are bit lines," where "each one of the pair of input transmission lines is coupled to another gate of the dual-gated MOSFET in each amplifer" (from independent claim 10 on which claim 13 depends).

In contrast, Austin describes bit lines coupled to gates of transistors 121, 124. *See, column 4, lines 61-63 and figure 1D.* The transistors 121, 124 are not the pair of cross-coupled transistors cited and relied upon in the Office Action as a disclosure with respect to the dual-gated MOSFET of claim 13. The structure of the circuit with bit lines as described by Austin is distinctly different from a circuit with gates of a dual-gated MOSFET coupled to bit lines. Therefore, Austin does not teach or suggest, even when combined with Chung, bit lines as recited in claim 13.

Claims 23, 29, 32, 35, 37, 40, 44, and 45 recite similar elements as claim 13 and are patentable over Austin in view of Chung. Consequently, claims that depend from these claims are patentable over Austin in view of Chung for the reasons stated above and the elements of the claims.

Accordingly, in view of these remarks, Applicant respectfully requests reconsideration and withdrawal of the 103 rejection for the above cited claims as well as all claims which depend therefrom.

It is noted that all of the claim rejections involve the Austin and Chung combination. Claims 28 and 40-43 were rejected under 35 USC § 103(a) as being unpatentable over Kaneko et al. (US 6,068,828 in view of Austin (U.S. 5,982,690) and Chung (U.S. 5,442,209). The Kaneko reference does not cure the deficiencies in the Austin and Chung combined references.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (612-373-6913) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 27th day of March, 2002.

Name Amy Moriarty Signature